# A Family of Low Cost High Performance HEMT MMICs for Commercial DBS Applications

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## Abstract

A family of GaAs HEMT MMICs have been developed for use in Direct Broadcast Satellite TV (DBS) US, Japanese, and European markets. These designs are very compact, high performance, and self-biased. They are meant as building blocks for low noise block (LNB) downconverters. Described in this paper are the receiver chip, low noise amplifier, and self-biased single HEMT device (should a MIC LNA be preferred). The key design is the receiver chip with a nominal gain of 38 dB and NF of less than 3 dB for the US band. This paper presents a description of each design, a performance summary, as well as information describing their actual use in an LNB design.

## Introduction

Present LNB designs utilize 2- or 3-stage discrete LNAs using packaged low-noise HEMTs and MESFET monolithic receivers. They typically follow a standard biasing approach which requires both positive and negative voltages.

Use of high-performance HEMT monolithic LNAs and receivers could greatly simplify LNB board layouts. Additionally, the lower noise and higher gain of a HEMT downconverter could lower the number of required LNA stages and/or provide superior performance over a similarly designed LNB utilizing a MESFET design.

Self-bias circuitry requires only a positive voltage source, resulting in fewer biasing components. This allows a simplified board layout and lower manufacturing cost. Self-bias design difficulties, such as instability at low frequencies, can be overcome. For example, low frequency stability can be improved through the use of frequency dependent RC networks which reduce out-of-band gain.

Cost advantages gained through high performance and self-bias HEMT MMIC would be lost if the resulting designs were large and space inefficient. Therefore, small size was a major goal. Risks of minimized size were taken at the onset of the develpment. Designs started out compact; no 1st generation large versions were attempted. Mixer and IF amplifier, DRO and Buffer Amp were designed as an integerated macrocell. No attempt was made to reach a 50 ohm interface, thereby reducing the amout of on-chip matching elements. Signal-ground (S-G) input and output pads were used instead of the more common G-S-G configuration. Odd-shaped capacitors with vias embedded in their structure were used. Complex structures were verified using EM simulation. The result of these actions were highly efficient, compact designs.

## Designs

The most challenging and critical design is the monolithic receiver. It consists of an 2-stage LNA, a dual-gate (DG) active mixer, a DRO and buffer



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amplifier, and a 2-stage IF amplifier shown schematically in Fig. 1.

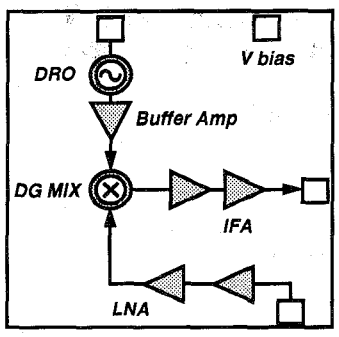


**Figure 1 - MMIC Receiver Block Diagram**

It is very compact design 1580um x 1460um, or 2.3 $mm^2$, as shown in Fig. 2.

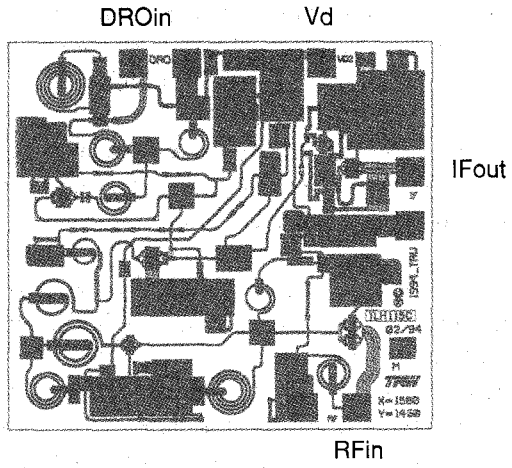


**Figure 2 - MMIC Receiver Layout**

Power requirements are drain voltage of 6 V and drain current of less than 125 mA. Designs were completed for 3-bands: US band (RF of 12.2 to 12.7 GHz), Japanese and High Astra band (RF of 11.7 to 12.5), and European and Low Astra band (10.7 to 11.8 GHz). Typical gain is from 38 to 40 dB with noise figures better than 3.5 dB. On-wafer measured gain and noise figure performance for each band is shown in Fig. 3 (US), Fig. 4 (Japan/Astra), and Fig. 5 (European).

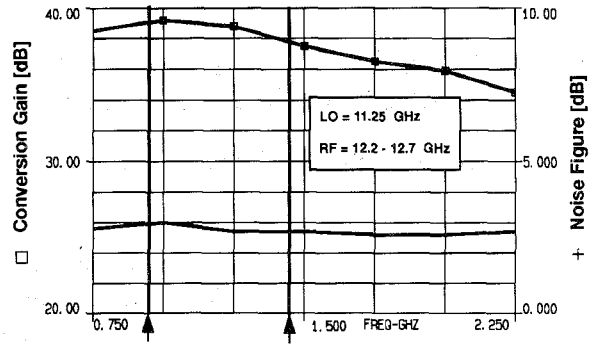


**Figure 3 - US Band MMIC Receiver**

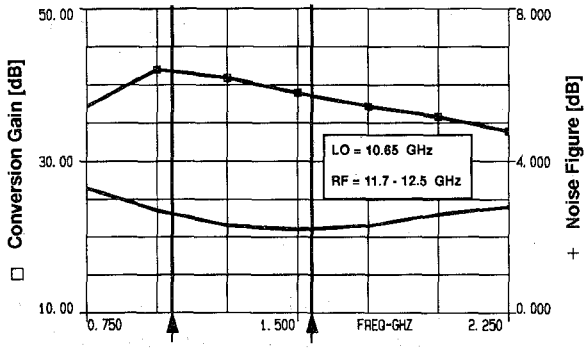


**Figure 4 - Japanese/High Astra Band MMIC Receiver**

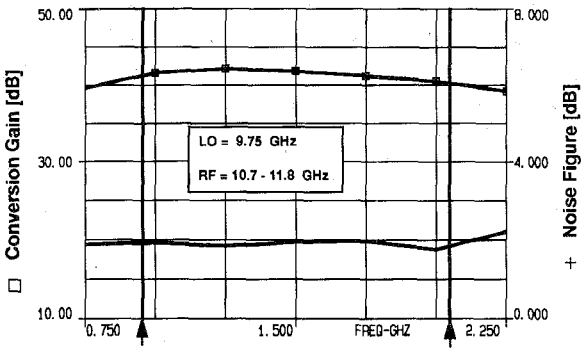


**Figure 5 - European Band MMIC Receiver**

This performance is significantly better than existing MESFET designs [1].

The LNA is similar to the stand-alone monolithic LNA (shown in Fig. 6) with the addition of resistive loading to provide unconditional stability. 1st stage utilized a 200 um 8 finger HEMT, chosen for ease of NF match, while the 2nd stage used 100-µm 4 finger HEMT chosen for low DC current. Nominal gain was

20 dB with a center band noise figure of 1.3 dB. See Fig. 6 for schematic.

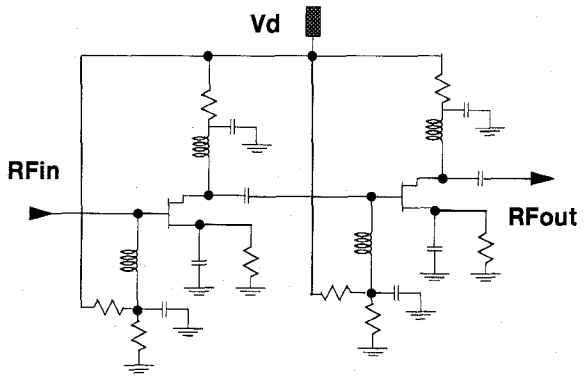


**Figure 6 - Self-Bias LNA Schematic**

The LNA drives an active 200-μm dual-gate mixer. The RF port of the mixer was matched to 50 ohms. No attempt was made to match the LO port. It had a 200-ohm resistor connected to the DG HEMT source virtual ground.

At the output of the mixer is a very compact 2-stage IF amplifier. It uses a 100-μm 1st stage and a 200-μm output stage for increased output drive. Larger devices were ruled out due to increased current consumption. Series resistors are used in both stages for stability. The output match is designed for a 75 ohm system. Gain of the mixer and IFA was 20 dB. It is important to note that, while the mixer and IFA were originally designed using nonlinear simulations, the stability of the IFA could be accurately predicted only through EM simulation.

The DRO and buffer amplifer use a 100-μm device for the oscillator and a 200-μm device for the buffer amplifier. The design was accomplished using both linear and non-linear Libra (using OSCTEST element). Initial conditions for oscillation were set first using linear simulation, and then fine tuned using the non-linear analysis. DRO input port has a postive s11 of approximately 6 dB, broadband enough for a single design meeting US and Japan LO needs. A second version meets the European LO needs. The buffer amplifier provides increased LO signal level and provides isolation between the DRO and the DG Mixer.

The individual LNA chip is designed to work with the receiver to provide a nominal 60 dB LNB gain block. Its area, as shown in Fig. 7, was not minimized. Its size is 860 μm x 1460 μm, using 1.3 $mm^2$. It was designed to allow the LNA and receiver chips to be placed side-by-side in a single package with LNA output and receiver input sharing a common side. .

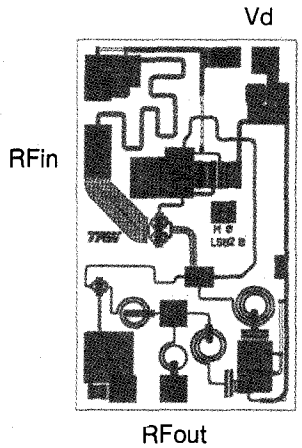


**Figure 7 - Self-Bias MMIC LNA Layout**

This allows the addition of an off-chip image-rejection filter. The circuit topology is similar the monolithic receiver LNA, though optimized for minimum noise figure. A tradeoff between stability and noise figure was made, resulting in worst case stability factor (k) of 1, an approximate gain of 20 dB, and a noise figure less than 1 dB. Wafer-probe data is shown in Fig. 8. This performance appears to comparable or slightly better than LNAs reported earlier [3].

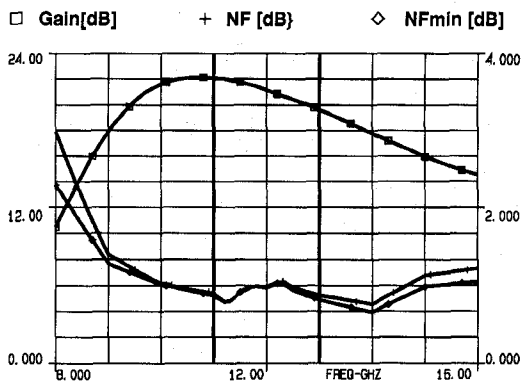


**Figure 8 - Self-Bias MMIC LNA**

Since many existing LNBs utilize MIC LNA designs for low cost and high performance, a single package HEMT device was designed to make a self-bias MIC LNA possible. A 200-μm 8-finger device with an embedded RC source structure was designed.

The schematic is shown in Fig. 9 and the layout is shown in Fig. 10.

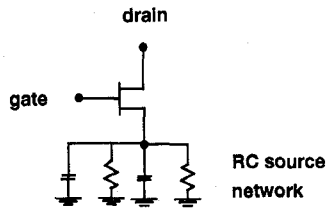


**Figure 9 - SBDEV Self-Bias HEMT Schematic**

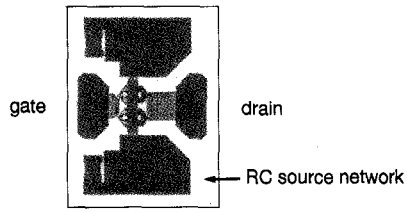


**Figure 10 - SBDEV Self-Bias HEMT Layout**

This results in a minimal source feedback, allowing the packaged HEMT to operate in a self-bias mode at 12 GHz. Off-chip resistors must be added to make the complete self-biased design. Test-fixture measured performance of a SBDEV in a 70 mil pill package is shown in Fig. 11. Ripple is due to test fixtures long transmission lines at input and output of DUT.

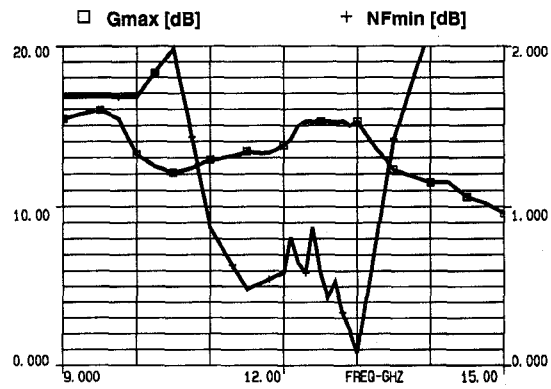


**Figure 11 - Self Bias HEMT**
**(Fixtured in a 70mil Pill Package)**

## Conclusion

A family of high-performance self-biased HEMT MMIC products have been demonstrated. All are very compact and achieve very high performance. Fig. 12 shows a typical LNB block diagram using these components. Work is continuing on optimizing the designs. Future MMIC receiver performance goals are gain greater than 40 dB and noise figure less than 2.5 dB.

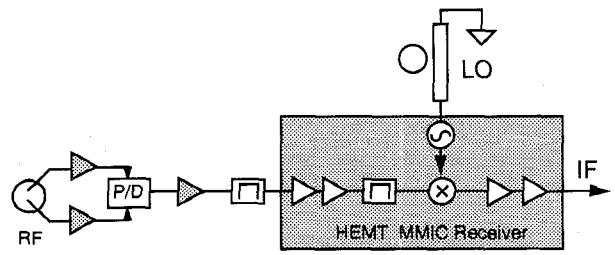


**Figure 12 - LNB Block Diagram**

## Acknowledgement

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## References

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